CLAIMS

I claim:

1. An integrated device comprising a high-voltage resistor integrated in a semiconductor material body wherein said high-voltage resistor has a vertical current flow structure.

2. An integrated device according to claim 1 wherein said high-voltage resistor has conductivity of the same type as that of said semiconductor material body.

3. An integrated device according to claim 1 wherein said high-voltage resistor is formed by a portion of said semiconductor material body extending between a first and a second surface of the semiconductor material body, and delimited at least partially by an insulation region extending from said first surface towards said second surface of said semiconductor material body.

4. An integrated device according to claim 3 wherein said insulation region has a closed shape in plan view.

5. An integrated device according to claim 3 wherein said insulation region is formed entirely of isolating material.

6. An integrated device according to claim 3, further comprising a first and a second region having conductivity opposite that of said semiconductor material body, and arranged on opposite sides of said insulation region.

7. An integrated device according to claim 1, further comprising first and second electronic devices formed in said semiconductor material body on opposite sides of said insulation region.

8. A process for manufacturing an integrated device that includes a high-voltage resistor, the method comprising:

forming a semiconductor material body; and

forming in a said semiconductor material body a high-voltage resistor having a vertical current flow structure.

9. A manufacturing process according to claim 8 wherein forming a high-voltage resistor comprises the step of:

forming in said semiconductor material body an insulation region extending from a first surface towards a second surface of the semiconductor material body, and delimiting at least partially a portion of said semiconductor material body.

10. A manufacturing process according to claim 9 wherein said insulation region has a closed shape in plan view.

11. A manufacturing process according to claim 9 wherein forming an insulation region comprises:

forming a trench having a closed shape in plan view; and

filling said trench with an insulating material.

12. A manufacturing process according to claim 11 wherein filling said trench comprises the step of forming an oxide layer filling said trench completely.

13. A manufacturing process according to claim 11 wherein said step of filling said trench comprises the steps of:

forming an oxide layer covering lateral walls and a base wall of said trench, and filling the trench partially; and

filling the remaining part of said trench with an insulating material.

14. A manufacturing process according to claim 9, further comprising:

forming in said semiconductor material body, a first and a second buried region spaced from one another and having a type of conductivity opposite that of the semiconductor material body; wherein said insulation region is arranged between said first and second buried regions and extends in depth beyond the first and second buried regions.

15. A manufacturing process according to claim 9, further comprising:

forming in the portion of said semiconductor material body surrounded by said insulation region, and at said first surface, a region with low resistivity and having the same type of conductivity as said semiconductor material body.

16. A manufacturing process according to claim 9, further comprising:

forming in the portion of said semiconductor material body surrounded by said region of isolation, and at said first surface, a region with low resistivity and having conductivity of the type opposite that of said semiconductor material body.

17. A process for manufacturing an integrated device comprising a high-voltage resistor, the method comprising:

forming a semiconductor material body;

forming in said semiconductor material body a buried region having conductivity opposite that of the semiconductor material body;

forming a trench having a closed shape in plan view;

forming an oxide layer covering the lateral walls and the base wall of said trench; and

filling a remaining part of said trench with a conductive material.

18. A manufacturing process according to claim 17, further comprising:

forming in the portion of said semiconductor material body surrounded by said trench, and at said first surface, a first region with low resistivity and having the same type of conductivity as said semiconductor material body.

19. A manufacturing process according to claim 17, further comprising:

forming in the portion of said semiconductor material body surrounded by said trench, a second region having the same type of conductivity as said buried region.

20. An integrated device, comprising:

a semiconductor body having a surface;

a doped semiconductor region extending longitudinally into the semiconductor body from the surface, the semiconductor region being a resistor extending transversely with respect to the surface; and

an insulating region extending longitudinally into the semiconductor body from the surface, the insulating region laterally surrounding the semiconductor region.

21. The device of claim 20 wherein the insulating region is open at a bottom portion such that the semiconductor region is contiguous with the semiconductor body.

22. The device of claim 20 wherein the semiconductor region has a rectangular cross-section and the insulating region has a rectangular frame shape.

23. The device of claim 20 wherein the insulating region is completely of electrically isolating material.

24. The device of claim 20 wherein the insulating region includes insulating walls made of electrically insulating material and a conductive filler that is laterally surrounded by the insulating walls.

25. The device of claim 24 wherein the semiconductor region includes an upper region of a first conductivity type; a middle region of a second conductivity type, opposite to the first conductivity type; and a lower region of the first conductivity type, the middle region being positioned between the upper and lower regions such that a transistor is formed that

includes the conductive filler as a gate, the upper region as a first source/drain, and the lower region as a second source/drain.

26. The device of claim 20, further comprising first and second semiconductor regions having conductivity opposite to a conductivity of the semiconductor material body, and arranged immediately adjacent to opposite sides of the insulation region.

27. The device of claim 20 wherein the semiconductor region includes an upper region adjacent to the surface of the semiconductor body and a lower region positioned below the upper region, the upper region being doped at a higher doping level compared to the lower region.

28. The device of claim 20 wherein the semiconductor region includes an upper region adjacent to the surface of the semiconductor body and a lower region positioned below the upper region, the upper region having a conductivity type opposite to a conductivity type of the lower region, thereby forming a diode.